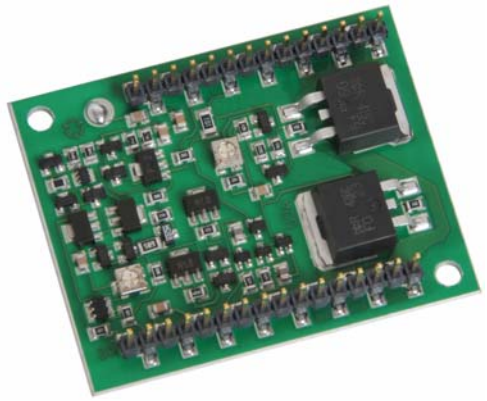
PowerAmp Design

POWER OPERATIONAL AMPLIFIER PAD39

Rev B

KEY FEATURES

- **HIGH VOLTAGE – 100 VOLTS**
- **HIGH CURRENT – 10 AMPS**
- **125 WATT DISSIPATION CAPABILITY**
- **HIGH SLEW RATE- 10V/µS**
- **FOUR WIRE CURRENT LIMIT**
- **OPTIONAL BOOST VOLTAGE INPUTS**



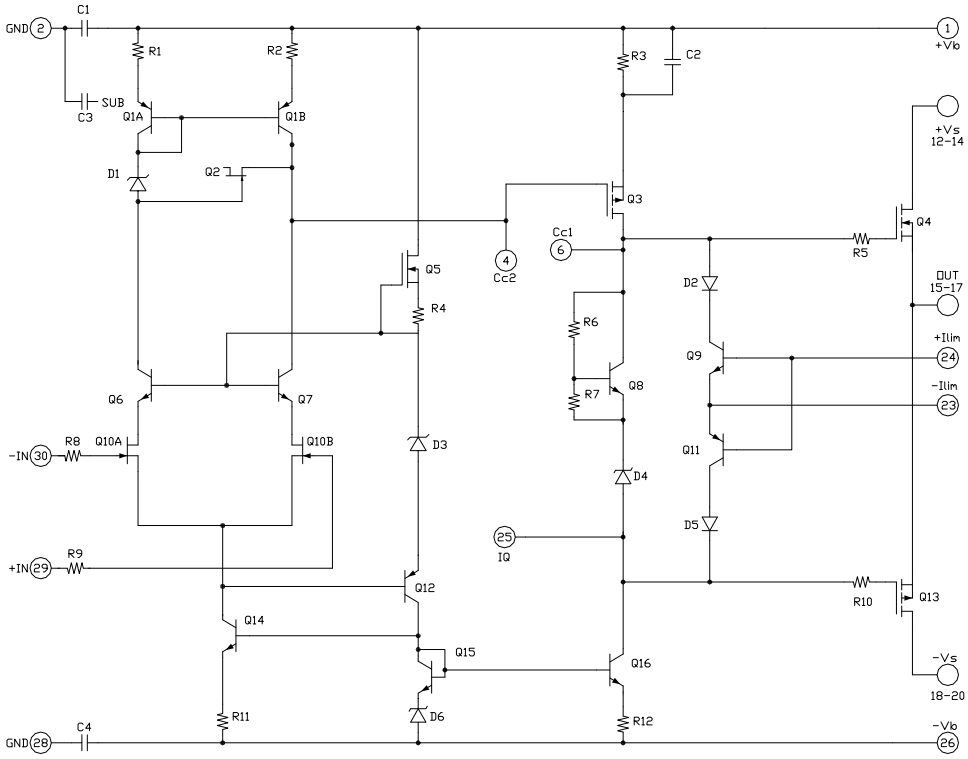
APPLICATIONS

- **LINEAR AND ROTARY MOTOR DRIVE**
- **YOKE/MAGNETIC FIELD EXCITATION**
- **PROGRAMMABLE POWER SUPPLIES**
- **INDUSTRIAL (PA) AUDIO**

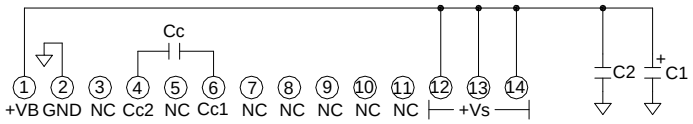
DESCRIPTION

The PAD39 is a power operational amplifier constructed with surface mount components to provide a cost effective solution for many industrial applications With a footprint only 3.3in^2 the PAD39 offers outstanding performance that rivals more expensive hybrid component amplifiers or rack-mount amplifiers. User selectable external compensation tailors the amplifier's response to the application requirements. Programmable current limit is built-in. The amplifier circuitry is built on a thermally conductive but electrically insulating substrate. No BeO is used in the PAD39. The resulting module is a small, high performance solution for many industrial applications.

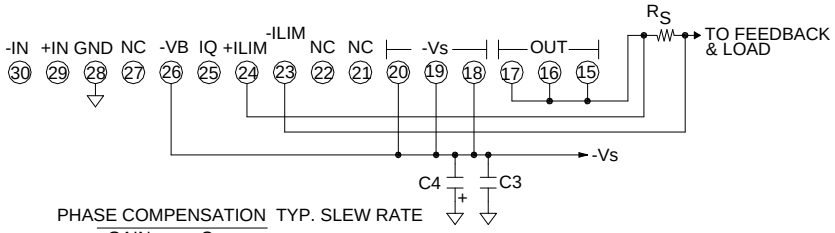
EQUIVALENT CIRCUIT



PINOUT & CONNECTIONS



VIEW FROM COMPONENT SIDE



PHASE COMPENSATION		TYP. SLEW RATE
GAIN	Cc	
1	470pF	4V/uS
3	220pF	9V/uS
≥ 5	100pF	15V/uS
≥ 12	47pF	20V/uS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, +Vs to −Vs	100V	TEMPERATURE, pin solder, 10s	200C
BOOST VOLTAGE,	±Vs ±20V	TEMPERATURE, junction[2]	175°C
OUTPUT CURRENT, within SOA	25A	TEMPERATURE RANGE, storage	−40 to 105°C
POWER DISSIPATION, internal, DC	125W	OPERATING TEMPERATURE, case	−40 to 105°C
INPUT VOLTAGE, differential	± 20V		
INPUT VOLTAGE, common mode	$\pm V_B$		

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE			1	3	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		20	50	µV/°C
OFFSET VOLTAGE vs. supply				20	µV/V
BIAS CURRENT, initial[3]				100	pA
BIAS CURRENT vs. supply				0.1	pA/V
OFFSET CURRENT, initial				50	pA
INPUT RESISTANCE, DC			100		G Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE				$+V_B-15$	V
COMMON MODE VOLTAGE RANGE				$-V_B+7$	V
COMMON MODE REJECTION, DC		98	106		dB
NOISE	100kHz bandwidth, 1kΩ R_S		10		µV RMS
GAIN					
OPEN LOOP	R_L= 10kΩ, C_C=100pF	108			dB
GAIN BANDWIDTH PRODUCT @ 1MHz	C_C=100pF		2		MHz
PHASE MARGIN	Full temperature range	45	60		degree
OUTPUT					
VOLTAGE SWING	I_O = 10A	±Vs−8	+Vs−6.6		V
VOLTAGE SWING	I_O = −10A	−Vs+7	−Vs+6		V
VOLTAGE SWING	$+V_B$=+Vs+10V, I_O = 10A	+Vs−2	+Vs−1.2		
VOLTAGE SWING	$-V_B$=-Vs-10V, I_O = -10A	-Vs−2.8	+Vs+2.2		
CURRENT, continuous, DC			10	11	A
SLEW RATE, A_V = −10	C_C = 100pF	10	15		V/µS
SETTLING TIME, to 0.1%	2V Step, C_C = 100pF		2.5		µS
RESISTANCE	No load, DC		4		Ω
POWER SUPPLY					
VOLTAGE		± 15	± 40	± 50	V
CURRENT, quiescent, boost supply				22	mA
CURRENT, total				26	mA
THERMAL					
RESISTANCE, AC, junction to air[5]	Full temperature range, f ≥ 60Hz			0.9	°C/W
RESISTANCE, DC junction to air, outputs	Full temperature range			1.2	°C/W
TEMPERATURE RANGE, heat sink		−40		105	°C

NOTES:
1. Unless otherwise noted: T_C = 25°C, compensation Cc = 470pF, DC input specifications are ± value given, power supply voltage is typical rating.
2. Derate internal power dissipation to achieve high MTBF.
3. Doubles for every 10°C of case temperature increase.
4. +Vs and −Vs denote the positive and negative supply voltages to the output stage. $+V_B$ and $-V_B$ denote the positive and negative supply voltages to the input stages.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
7. Power supply voltages $+V_B$ and $-V_B$ must not be less than +Vs and −Vs respectively. Total voltage $+V_B$ to $-V_B$ 120V maximum.
8. The PAD39 is constructed with MOSFET transistors and ESD handling procedures must be observed.

SAFETY FIRST

The operating voltages of the PAD39 are potentially deadly. When developing an application circuit it is wise to begin with power supply voltages as low as possible while checking for circuit functionality. Increase supply voltages slowly as confidence in the application circuit increases. Always use a "hands off" method whereby test equipment probes are attached only when power is off.

CURRENT LIMIT

The current limiting function of the PAD39 is a versatile circuit that can be used to implement a four-wire current limit configuration. The four-wire current limit configuration insures that parasitic resistance in the output line, Rp, does not affect the programmed current limit setting. See Figure 1 below. The sense voltage for current limit is 0.7V. Thus:

$$I_L = \frac{0.7V}{R_s}$$

Where I_L is the value of the limited current and R_S is the value of the current limit sense resistor.

In addition, the sense voltage has a temperature coefficient approximately equal to −2.2mV/°C.

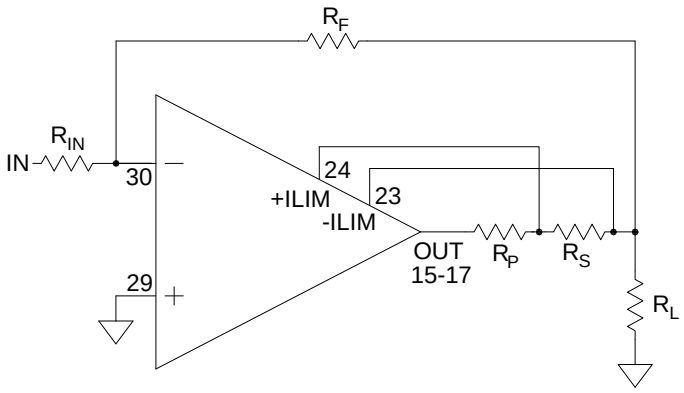


Figure 1

MOUNTING THE AMPLIFIER

In most applications the amplifier must be attached to a heat sink. Spread a thin and even coat of heat sink grease across the back of the PAD39 and also the heat sink where the amplifier is to be mounted. Push the amplifier into the heat sink grease on the heat sink while slightly twisting the amplifier back and forth a few times to bed the amplifier into the heat sink grease. On the final twist align the mounting holes of the amplifier with the mounting holes in the heat sink and finish the mounting using 4-40 hex male-female spacers. Mount the amplifier to the mother board with 4-40 X 1/4" screws.

PHASE COMPENSATION

The PAD39 **must** be phase compensated. The compensation capacitor, C_C, is connected between pins 4 and 6. The compensation capacitor must be an NPO type capacitor rated for the full supply voltage (100V). On page 2, under Amplifier Pinout and Connections, you will find a table that gives recommended compensation capacitance value for various circuit gains and the resulting slew rate for each capacitor value. Consult also the small signal response and phase response plots for the selected compensation value in the Typical Performance Graphs section. A compensation capacitor less than 100pF is not recommended.

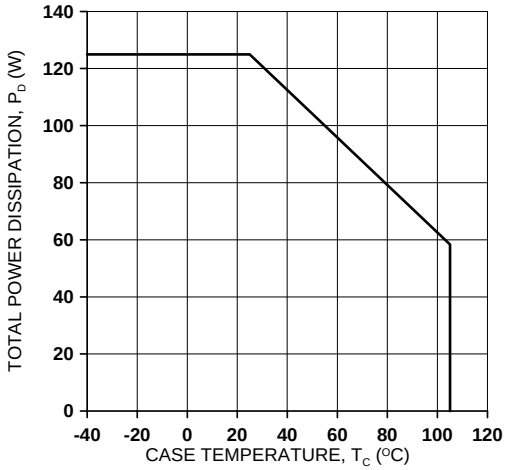
USING THE IQ PIN FUNCTION

When pin 25 (IQ) is tied to pin 6 (Cc1) the class AB bias of the output stage becomes C bias. The quiescent current of the PAD39 typically drops by 10mA. In some applications the reduced quiescent current is important. However, note that applying this option will raise the output impedance of the amplifier which may change the stability of the circuit and will also increase crossover distortion.

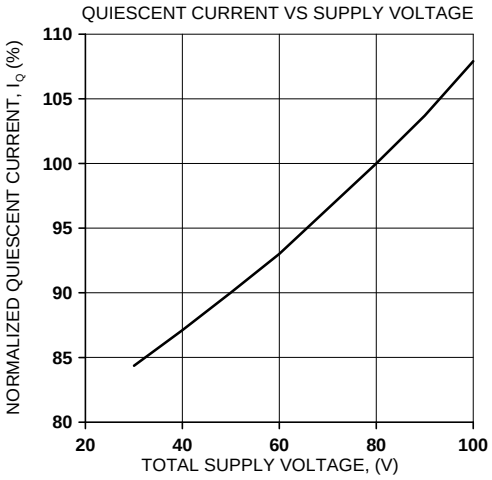
BOOST OPERATION

The small signal stages of the PAD39 are connected to the $\pm V_B$ power supply pins. When the $\pm V_B$ voltages are greater than the ±Vs power supply pins the small signal stages of the amplifier are biased so that the output transistors can be driven very close to the ±Vs rails. Close swings to the supply rails increase the efficiency of the amplifier and make better use the supply voltages. This technique is often used to operate the amplifier with only a single high current power supply, thus reducing the system size and cost.

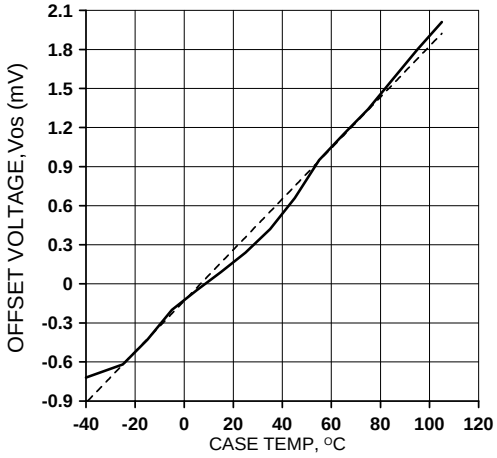
POWER DERATING



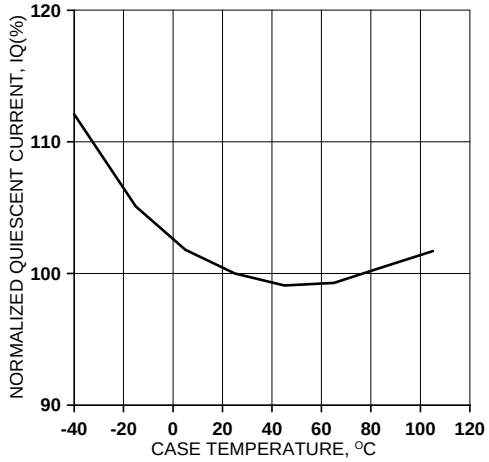
QUIESCENT CURRENT VS SUPPLY VOLTAGE



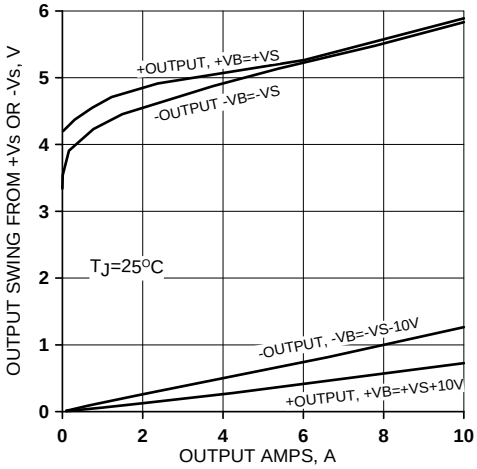
OFFSET VOLTAGE DRIFT



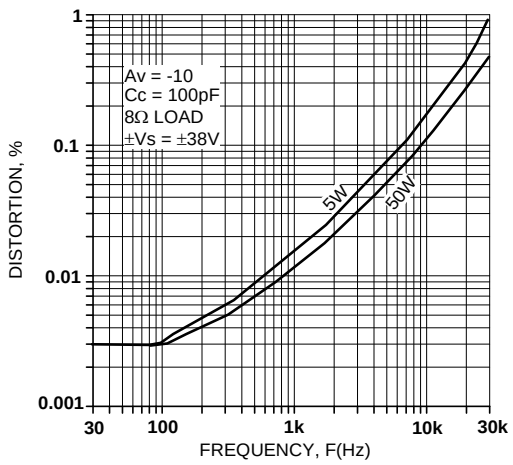
QUIESCENT CURRENT VS TEMPERATURE



OUTPUT SWING FROM SUPPLY RAILS



HARMONIC DISTORTION



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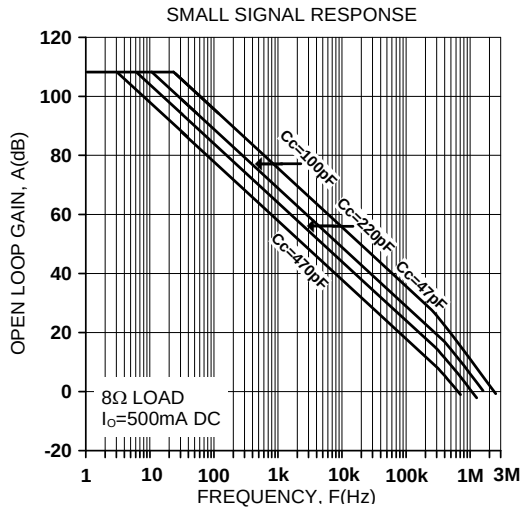
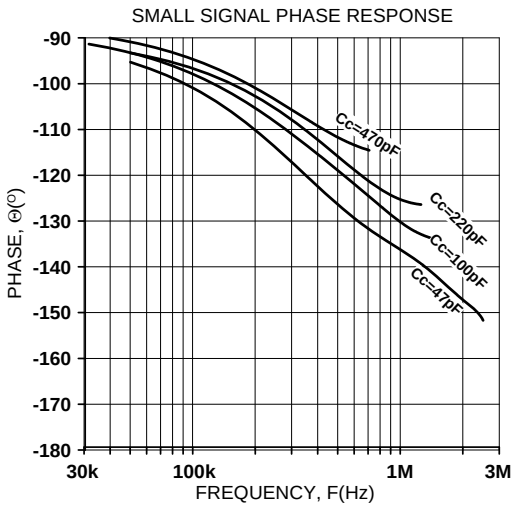
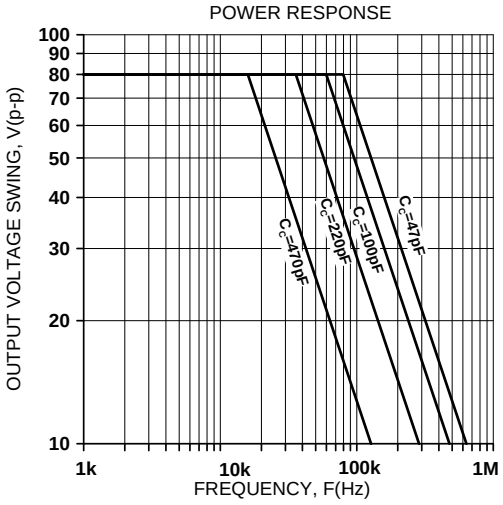
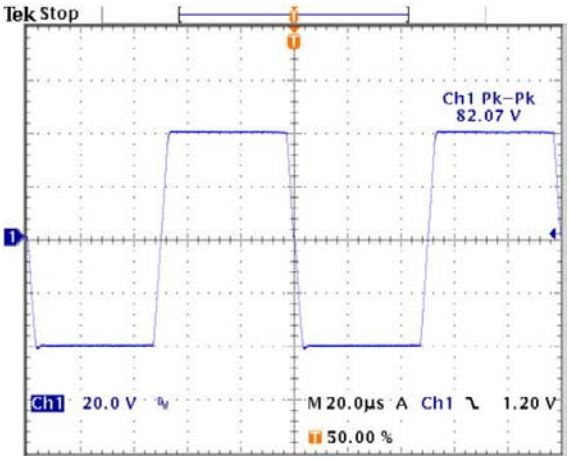
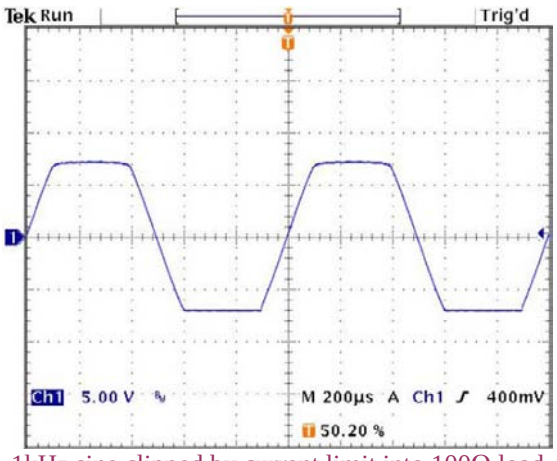




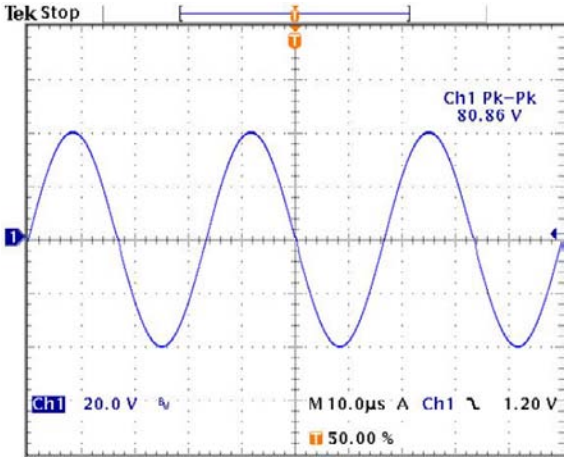




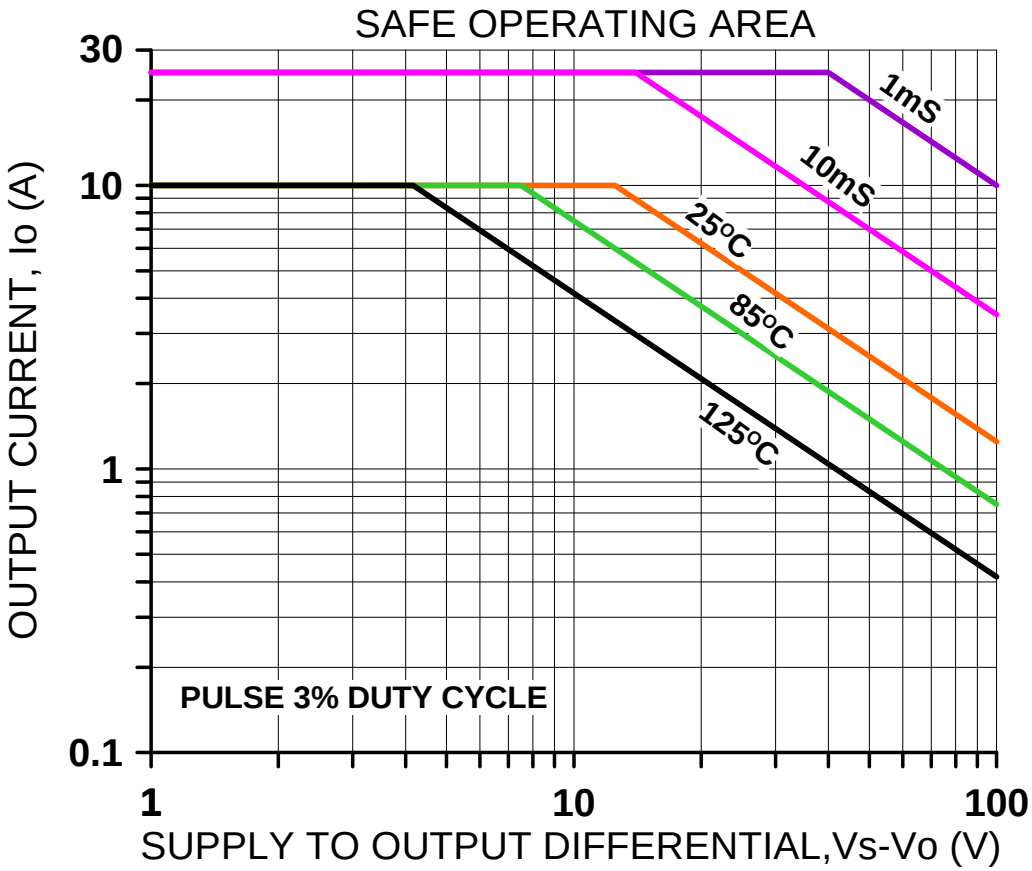
10kHz square into 8Ω load, G= −10,C_C=100pF, Vs=±50V



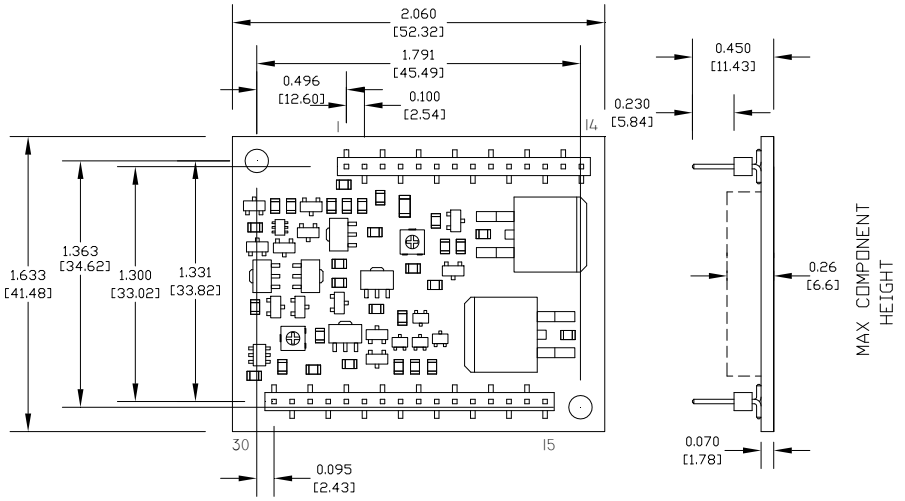
1kHz sine clipped by current limit into 100Ω load



30kHz sine into 8Ω load, G= −10,C_C=100pF, Vs=±50V



SAFE OPERATING AREA



NOTES: 1: DIMENSIONS ARE INCHES, [mm]
2: PINS 0.025" SQUARE [0.635mm], GOLD PLATED
3: RECOMMENDED HOLE FOR MOUNTING 0.129" D. x2 [3.277mm]
4: RECOMMENDED HOLE FOR PINS 0.052" D. [1.321mm]
5: HIGHLY RECOMMENDED THAT AMPLIFIER IS MOUNTED INTO CAGE JACKS USING PAD PART NUMBER CJS01. USE 0.062" [1.575mm] HOLE FOR CAGE JACKS.
6: HIGHLY RECOMMENDED THAT AMPLIFIER IS MOUNTED INTO HEAT SINK WITH 4-40 M/F SPACERS TO PROVIDE STRAIN RELIEF FOR PINS. SEE DRAWING BELOW.